

3 a silicon chip having I/O pads;

A4  
cont  
6 an under-ball metallurgy (UBM) layer on the surface of  
said I/O pads;

a substrate having a thickness between about 150 to 300  $\mu\text{m}$   
9 adhered to an adhesive having a thickness between about 10  
to 100  $\mu\text{m}$  to form an adsubstrate, the adsubstrate having  
openings corresponding to the locations of said I/O pads;  
12 and

ball mountings formed over said adsubstrate and reaching  
15 said UBM layer over said I/O pads on said chip.

A5  
3. The CSP of claim 1, wherein said UBM layer comprises  
nickel or copper.

3

✓  
Please cancel claim 6.

A4  
11. A method of forming a chip scale package (CSP)  
comprising the steps of:

3

MEG2000-012

providing one or more chips having I/O pads with UBM layer  
on the surface of said I/O pads;

6

providing a substrate having a thickness between about 150  
to 300  $\mu\text{m}$ ;

9

applying an adhesive layer with a thickness between about  
10 to 100  $\mu\text{m}$  over said substrate, thus forming an  
adsubstrate composite;

Ab  
cont.

12

forming openings in said adsubstrate composite to match the  
spacing of corresponding said I/O pads of said chip;

15

attaching said chip(s) on said adsubstrate composite  
wherein said I/O pads of said chip(s) are placed on the  
corresponding openings on said adsubstrate composite to  
form a package;

21

forming a molding material around said package;

24

performing ball mounting over said openings on said  
adsubstrate of said package; and

27

sawing said substrate to form said CSP.

Claims 16 and 18, please cancel. ✓

A7 26. A method of forming a chip scale package (CSP) comprising the steps of:

3

providing a wafer having a plurality of chip sites with I/O pads;

6

forming an under-ball metal (UBM) layer over said I/O pads;

9 forming an adhesive layer over said UBM layer on said wafer to form an adwafer, the adhesive layer having a thickness between about 10 to 100  $\mu\text{m}$ ;

12

forming openings in said adhesive layer on said adwafer to reach said I/O pads underlying said UBM layer;

15

die sawing said adwafer to form said chip scale package (CSP);

18

MEG2000-012

providing a substrate having openings corresponding to said  
I/O pads;

*A7  
cont.* <sup>21</sup>  
attaching said CSP with said adhesive to said substrate;  
and

<sup>24</sup>  
forming ball mountings on said openings on said substrate  
to attach to said I/O pads on said CSP.

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<sup>27</sup> ✓  
Claim 33 has been cancelled.

#### REMARKS

Claims 1-5, 7-15, 17, 19-32, and 34-41 remain in this  
application. Claims 1, 3, 11 and 26 have been amended, and  
claims 6, 16, 18 and 33 cancelled.

Examiner Patricia Costanzo is thanked for examining the  
present invention thoroughly.

The examiner is also thanked for having pointed out some  
ambiguities in the last four lines on page of the present  
application. Those lines have been corrected to state, in